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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/313,037	05/17/1999	LOUIS M. MELI	PHN-17.438	3381

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EXAMINER	
BAKER, PAUL A	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 11/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/313,037	MELI, LOUIS M.	
	Examiner	Art Unit	
	Paul A Baker	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 – 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Palowski US Patent 5,426,769 in view of Dallas Semiconductor "DS87C550 Product Preview".

In regards to claim 1, Palowski discloses an instruction execution unit having an instruction set that contains a memory access instruction in table 3, execution of the memory access instruction causing the instruction execution unit to issue memory access signals with an access address determined from the currently selected address table 3 mov instructions producing signals in figure 10 states 2-4 on port 2; and

a control register that is instruction-settable in column 14 line 59 to respective control states that control whether or not the processing device updates the at least two addresses as a side-effect of executing the memory access instruction in the second table in column 15 (in comparison to first table).

Palowski does not disclose a register circuit for storing at least two addresses in parallel;

an address selector arranged to cycle a set of states in which respective ones of the at least two addresses become a currently selected address respectively;

or the execution of the memory access instruction further causing the address selector to cycle to a next one of the states.

Dallas Semiconductor discloses a register circuit for storing at least two addresses in parallel in Figure 1 elements DPTR0 and DPTR1,

an address selector (data pointer select bit SEL page 13 4th paragraph) arranged to cycle a set of states in which respective ones of the at least two addresses become a currently selected address respectively on page 14 first paragraph,

and execution of the memory access instruction further causing the address selector to cycle to a next one of the states on page 14 first paragraph and table of assembly code.

Palowski discloses in column 5 line 62 through column 6 line 2 that reducing the number of clock cycles required for external data access is desirable and a stated goal of Palowski. Dallas Semiconductor states on page 14, first column 3rd paragraph that the incorporation of two data pointer registers improves the efficiency of data moves. This efficiency is accomplished by eliminating the need to continually having to load the single DPTR register of the native 8051 architecture with the source and destination addresses (Thereby reducing the number of clock cycles required for external data

access). This increases code density, and reduces the time required for each move operation. The combination of Palowski and Dallas, while modifying the same facet of the 8051 architecture, do so in such a way that the combination of the two does not alter the functionality of the other; therefore there is a reasonable expectation of success for the combination of the two prior art. Since Dallas Semiconductor states that the incorporation of two data pointer registers improves the efficiency of data moves, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate Dallas's shadow DPTR register in Palowski.

In regards to claim 2, Palowski further discloses each control state specifies respective update actions for all of the at least two addresses in column 14 lines 58 and 59.

In regards to claim 3, Palowski further discloses the control states specifying a choice of at least no-update, update by incrementing with a predetermined value and update by decrementing with the predetermined value in column 14 lines 61 – 65.

In regards to claim 4, Palowski further discloses that execution of the memory access instruction further causes the instruction execution unit to perform, upon the currently selected address, the update action that is specified by the control state of the control register for that one of the at least two addresses that is the currently selected address in column 15 lines 26 – 28.

In regards to claim 5, Palowski further discloses the instruction set includes a load from memory instruction and store to memory instruction, for causing the execution unit to respond ro the execution the memory access instruction in column 15 lines 22 – 25.

In regards to claims 6 and 7, according to last submitted copy of claims filed 10 February 2003, no copy of claim 6 or 7 is provided. Since first examining this case, the record has been translated from a paper record to an electronic format. The examiner cannot find anywhere in the electronic record where applicant has explicitly withdrawn claims 6 and 7 from consideration. The examiner can only infer that the applicant wishes to do so through the omission of claims 6 and 7 from the presented claims. For the sake of completeness the examiner has included rejection of claims 6 and 7. It is requested that if the applicant has withdrawn claims 6 and 7 from consideration, to explicitly state so in their next response and to disregard the following two rejections.

In regards to claim 6, Applicant discloses as prior art a program for executing alternately the load from memory instruction and the store to memory instruction, for an address addressed by a first one and a second one of the at least two addresses respectively on page 2 lines 6 and 7. Applicant does not disclose the setting the control register to one of the control states that causes both the first one and second one of the address to be updated. Palowski discloses the enable and disable for the auto-

increment/auto-decrement may be set individually in column 14 lines 63-65. Since the combination of Palowski and Dallas would provide a system, that once set up, would provide source to destination data moves consisting of alternate "move source to register" and "move register to destination" instructions (with no ancillary instructions), it would have been obvious at the time of invention to one of ordinary skill in the art to set both auto-updates for the purpose of moving blocks of data from one memory region to another memory region.

In regards to claim 7, Applicant discloses as prior art a program for executing alternately the load from memory instruction and the store to memory instruction, for an address addressed by a first one and a second one of the at least two addresses respectively on page 2 lines 6 and 7. Applicant does not disclose the setting the control register to one of the control states that causes only one of the first one and second one of the address to be updated. Palowski discloses the enable and disable for the auto-increment/auto-decrement may be set individually in column 14 lines 63-65. Since the combination of Palowski and Dallas would provide a system, that once set up, would provide source to destination data moves consisting of alternate "move source to register" and "move register to destination" instructions (with no ancillary instructions), it would have been obvious at the time of invention to one of ordinary skill in the art to set only one of the auto-updates for the purpose of transferring blocks of data to and from a memory mapped IO port.

In regards to claim 8, Dallas Semiconductor further discloses the address selector cycles back and forth between states that select a first and second one of at least two addresses respectively on page 14, first paragraph.

In regards to claim 9, Palowski further discloses each of four pages having an address and data SFR, given Dallas Semiconductor's motivation of improved efficiency of data moves given on page 13, first paragraph of "Dual Data Pointer With Inc/Dec"; it would have been obvious at the time of invention to one of ordinary skill in the art to include additional address registers one for each extra address SFR in order to improve the efficiency of inter-page data transfers. By incorporation of Palowski within Dallas Semiconductor the user would be able to cycle through selected states of the address SFR with the ability of incrementing or decrementing each address.

In regards to claim 10, Palowski discloses an instruction execution unit having an instruction set that contains a memory access instruction in table 3, execution of the memory access instruction causing the instruction execution unit to issue memory access signals with an access address determined from the currently selected address table 3 mov instructions producing signals in figure 10 states 2-4 on port 2; and

a control register in communication with said register selector register and said control register being instruction-settable in column 14 line 59 to respective control states that control whether or not the processing device updates the at least two

addresses will be updated as a side-effect of executing the memory access instruction in the second table in column 15 (in comparison to first table).

Palowski does not disclose discloses a register circuit for storing at least two addresses in parallel;

an address selector including a register selector register and a logic circuit collectively arranged to cycle a set of states in which respective ones of the at least two addresses become a currently selected address respectively;

or the execution of the memory access instruction further causing the address selector to cycle to a next one of the states.

Dallas Semiconductor discloses a register circuit for storing at least two addresses in parallel in Figure 1 elements DPTR0 and DPTR1,

an address selector including a register selector register (data pointer select bit SEL page 13 4th paragraph) and a logic circuit (inherent to perform cycling operation between the two address pointers) collectively arranged to cycle a set of states in which respective ones of the at least two addresses become a currently selected address respectively on page 14 first paragraph,

and execution of the memory access instruction further causing the address selector to cycle to a next one of the states on page 14 first paragraph and table of assembly code.

Palowski discloses in column 5 line 62 through column 6 line 2 that reducing the number of clock cycles required for external data access is desirable and a stated goal of Palowski. Dallas Semiconductor states on page 14, first column 3rd paragraph that the incorporation of two data pointer registers improves the efficiency of data moves. This efficiency is accomplished by eliminating the need to continually having to load the single DPTR register of the native 8051 architecture with the source and destination addresses (Thereby reducing the number of clock cycles required for external data access). This increases code density, and reduces the time required for each move operation. The combination of Palowski and Dallas, while modifying the same facet of the 8051 architecture, do so in such a way that the combination of the two does not alter the functionality of the other; therefore there is a reasonable expectation of success for the combination of the two prior art. Since Dallas Semiconductor states that the incorporation of two data pointer registers improves the efficiency of data moves, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate Dallas's shadow DPTR register in Palowski.

Response to Arguments

The examiner has changed the rejection of applicant's claimed invention from Dallas in view of Palowski to Palowski in view of Dallas, since Dallas provides motivation for combination with Palowski. According to MPEP §1208.01, In re Kronig, 539 F.2d 1300, 1302-03, 190 USPQ 425, 426-27 (CCPA 1976) establishes "Where the statutory basis for the rejection remains the same, and the evidence relied upon in

support of the rejection remains the same, a change in the discussion of, or rationale in support of, the rejection does not necessarily constitute a new ground of rejection." Since the statutory basis (35 USC §103) is the same, the evidence (the combination of Palowski and Dallas, and the same sections of each prior art are relied upon for the rejection of applicant's claimed invention as in the prior office action) is the same, and the applicant has been provided an opportunity to respond to the examiner's rejection under 35 USC §103 using the combination of Palowski and Dallas; the transition from Dallas in view of Palowski to Palowski in view of Dallas does not constitute a new ground of rejection. Since examiner's rejection is not a new ground of rejection, this is a final rejection.

Applicant's arguments filed 06 October 2004 have been fully considered but they are not persuasive.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Applicant provides the argument: "More particularly, it is noted that both of the cited references are complex, lengthy documents, with the Dallas Semiconductor

document running to 47 pages of complex, detailed technical information, and the Palowski patent containing 11 pages of drawing and 24 columns of text." The examiner is unable to find any support within the MPEP for this argument, the length of prior art disclosures has no bearing on their applicability in the rejection of a claimed invention, whether the prior art is used in part or whole.

Examiner is uncertain why the applicant has claimed: "undue experimentation would be required to locate and apply a feature to obtain a particular advantage as disclosed and claimed by applicant." Undue experimentation pertains to the requirement of an applicant to provide a detailed disclosure sufficient to enable one of ordinary skill in the art to make and use the disclosed invention (as detailed under 35 USC §112). The examiner does not understand how this is relevant to applicant's argument of impermissible hindsight.

Applicant argues that sufficient motivation to combine Palowski and Dallas does not exist. In addition to as cited in supra, the desire to make computing systems more efficient in their operation is very well known in the art. Indeed, this is typically the primary motivation for invention in the computer arts. A more efficient computer completes operations in a shorter period of time, consumes less program space, and consumes less power per operation. This motivation is provided in Palowski in column 5 line 62 through column 6 line 2 where he states that by reducing the number of clock cycles required for accessing external data, the clock speed of the microcontroller may be reduced (reducing power consumption) without effecting performance. Palowski also states in column 3 lines 2-6 that reducing the number of instructions required for

accessing external memory provides a higher code density, thereby reducing program space requirements. Additionally, both Palowski and Dallas disclose features to accelerate data movement within an 8051 architecture (the same architecture applicant's claimed invention is embodied within). The movement of data in a computer system is the most used subset of instructions within a computer, therefore acceleration of this subset of instructions would provide the greatest performance to cost ratio. For all these reasons (including the motivation provided by Dallas used in the rejection under 35 USC §103) the combination of Dallas into Palowski would have been obvious to one of ordinary skill in the art at the time of invention.

Applicant argues that since Palowski became public record (via granting Palowski a patent for his claimed invention) several years before Dallas developed the DS87C550, and Dallas did not include Palowski's auto-increment/decrement function for data pointers within the DS87C550, that no motivation exists for their combination. The examiner is unable to find any support for this argument within the MPEP; 35 USC §103 states "if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." If a secondary reference contains the missing elements and provides sufficient motivation for combination according to the guidelines of *Graham v. John Deere Co.,* and the combination of the two references would have been obvious to a person having ordinary skill in the art at the time of invention, the rejection under 35 USC §103 is valid.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul A Baker whose telephone number is (571)272-4203. The examiner can normally be reached on M-F 10am-6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571)272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PB

Mano Padmanabhan
11/9/04

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER